TDS290" 89200860

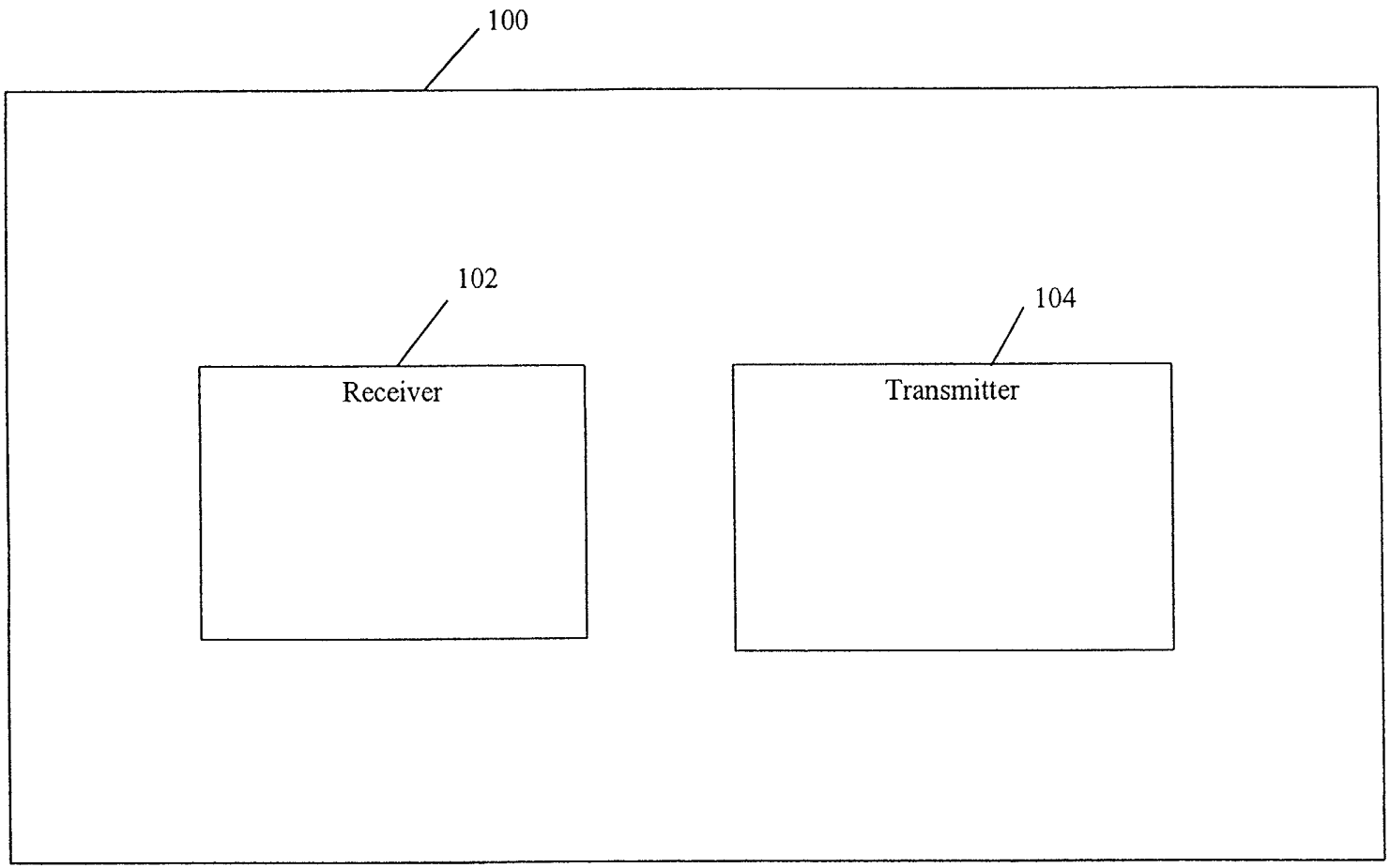


Figure 1

TDS290"89200860

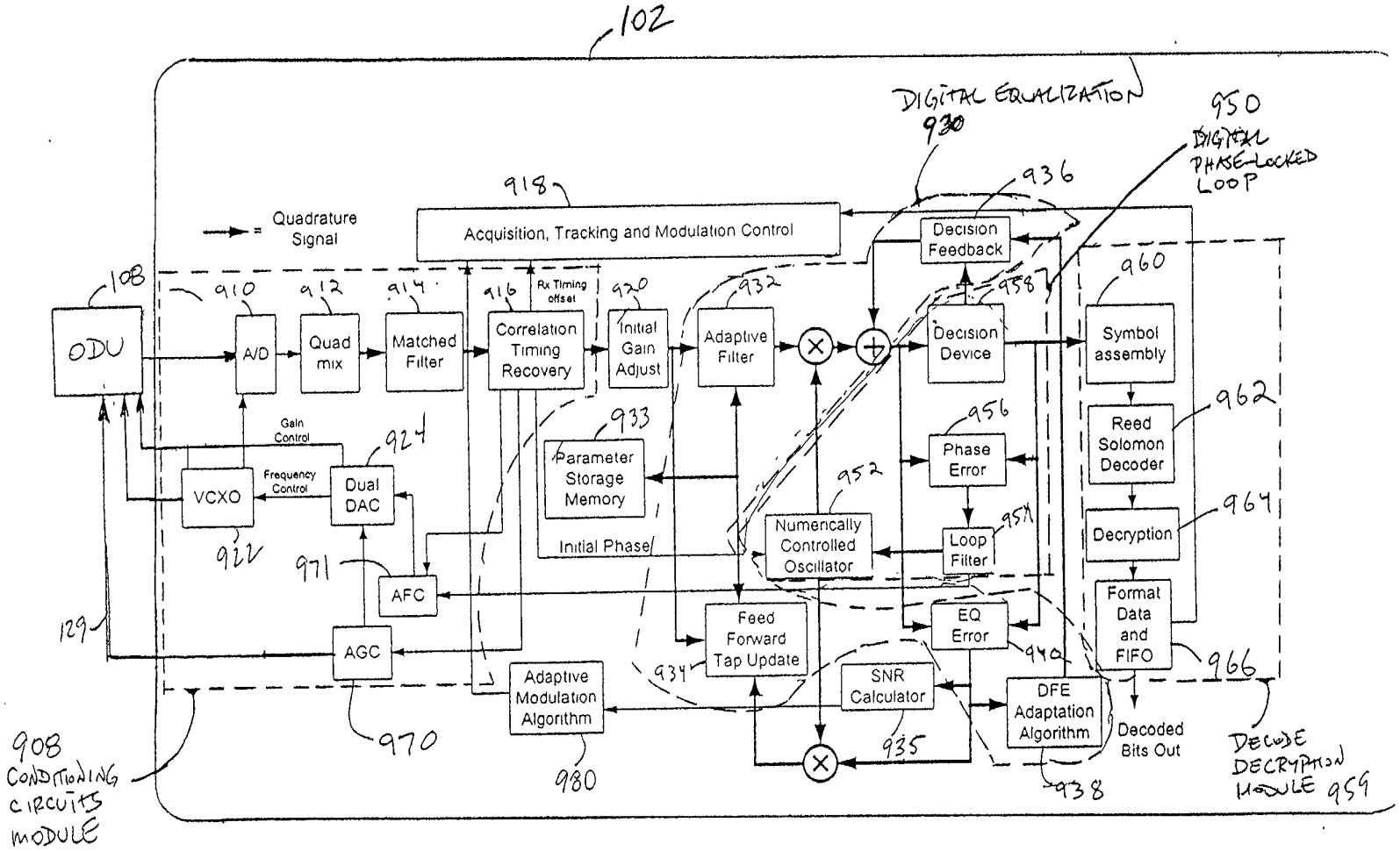


Figure 2

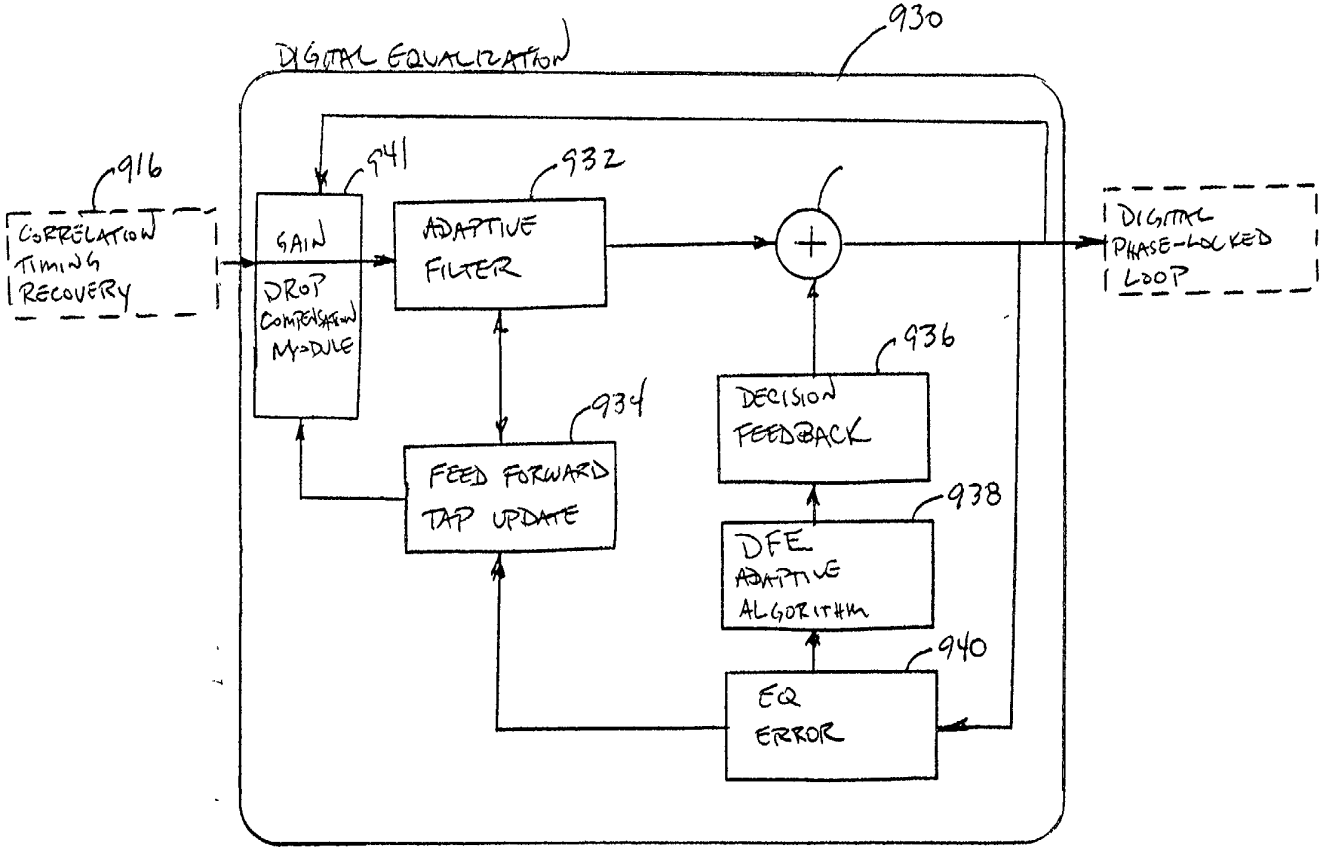

DIGITAL EQUALIZATION
930
916
CORRELATION TIMING RECOVERY
941
GAIN
DROP COMPENSATION MODULE
932
ADAPTIVE FILTER
DIGITAL PHASE-LOCKED LOOP
936
DECISION FEEDBACK
934
FEED FORWARD TAP UPDATE
938
DFE ADAPTIVE ALGORITHM
940
EQ ERROR

FIG. 3

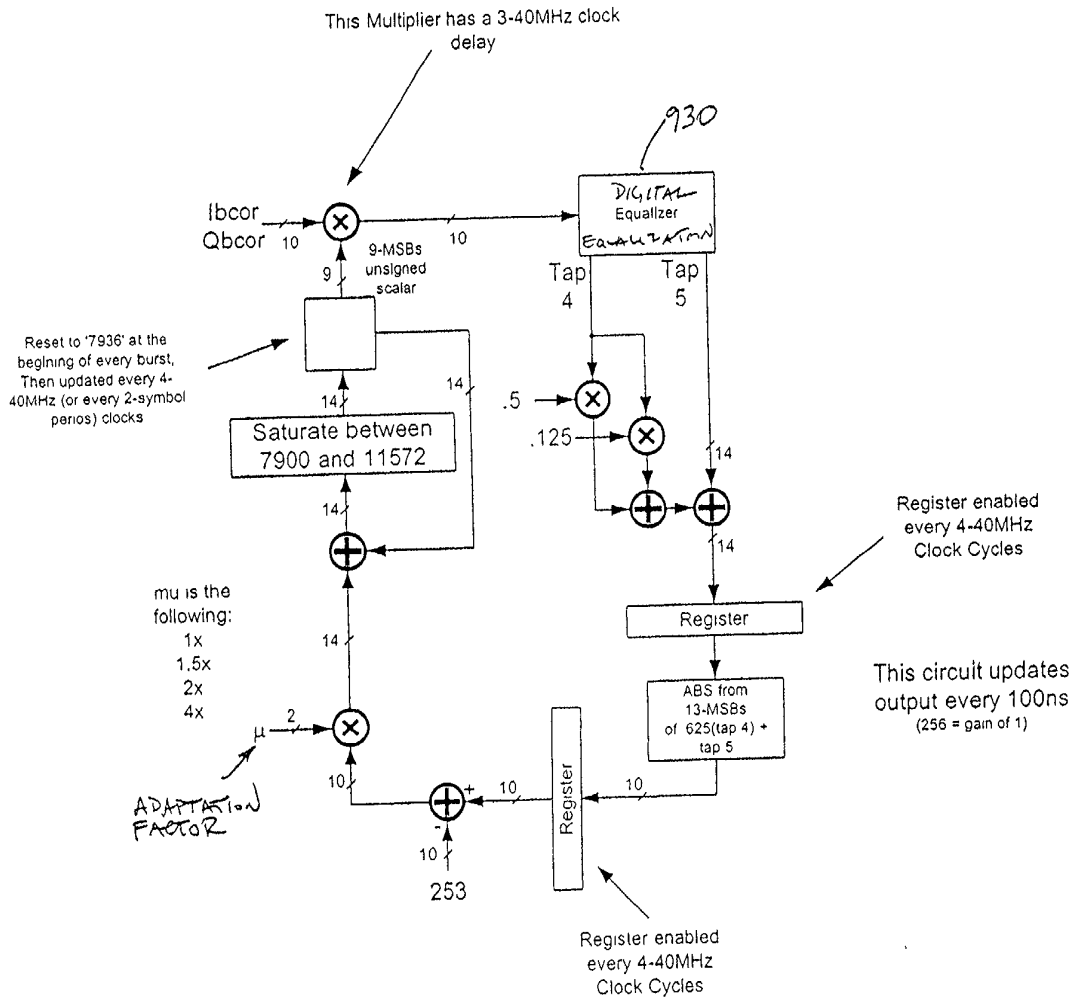

This Multiplier has a 3-40MHz clock delay
930
DIGITAL Equalizer
Ibcor
Qbcor
10
10
9
9-MSBs unsigned scalar
Tap 4
Tap 5
Reset to '7936' at the beginning of every burst, Then updated every 4-40MHz (or every 2-symbol perios) clocks
14
14
Saturate between 7900 and 11572
.5
.125
14
14
14
Register enabled every 4-40MHz Clock Cycles
Register
mu is the following:
1x
1.5x
2x
4x
14
ABS from 13-MSBs of 625(tap 4) + tap 5
This circuit updates output every 100ns
(256 = gain of 1)
2
μ
ADAPTATION FACTOR
10
10
10
Register
10
253
Register enabled every 4-40MHz Clock Cycles

FIGURE 4

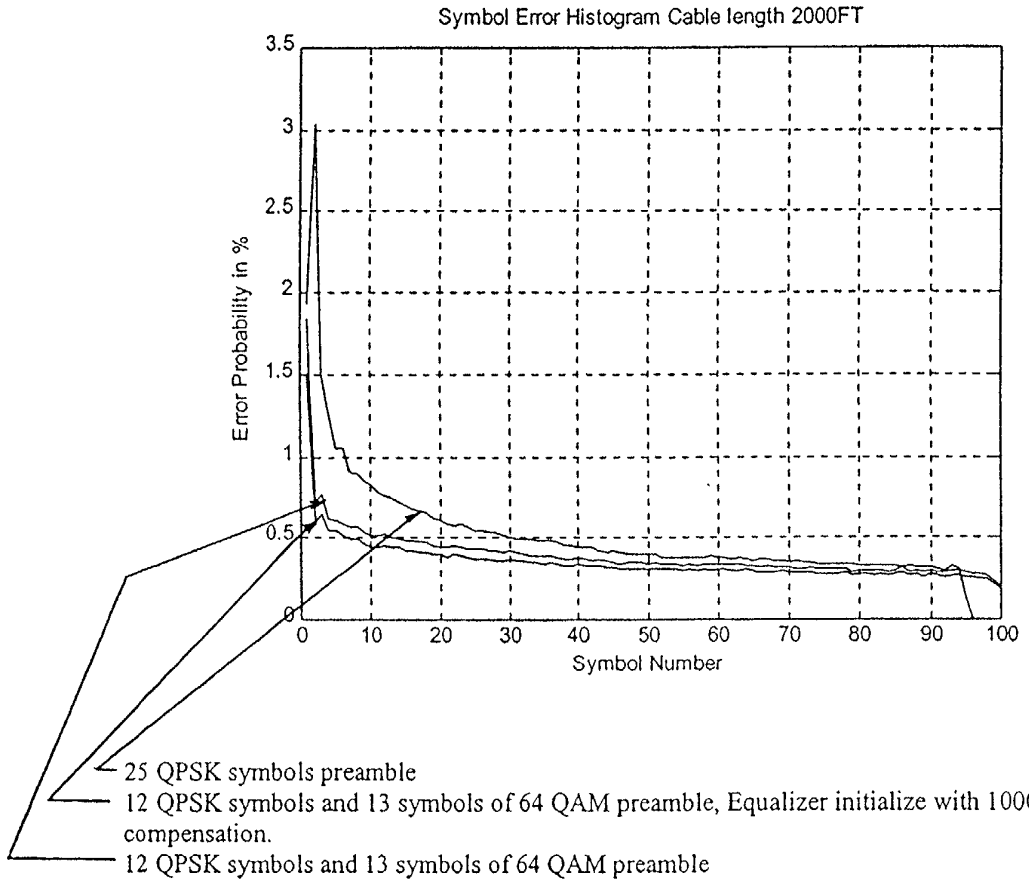

Symbol Error Histogram Cable length 2000FT
Error Probability in %
Symbol Number
3.5
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
80
90
100
25 QPSK symbols preamble
12 QPSK symbols and 13 symbols of 64 QAM preamble, Equalizer initialize with 1000FT-cable compensation.
12 QPSK symbols and 13 symbols of 64 QAM preamble

Figure 5

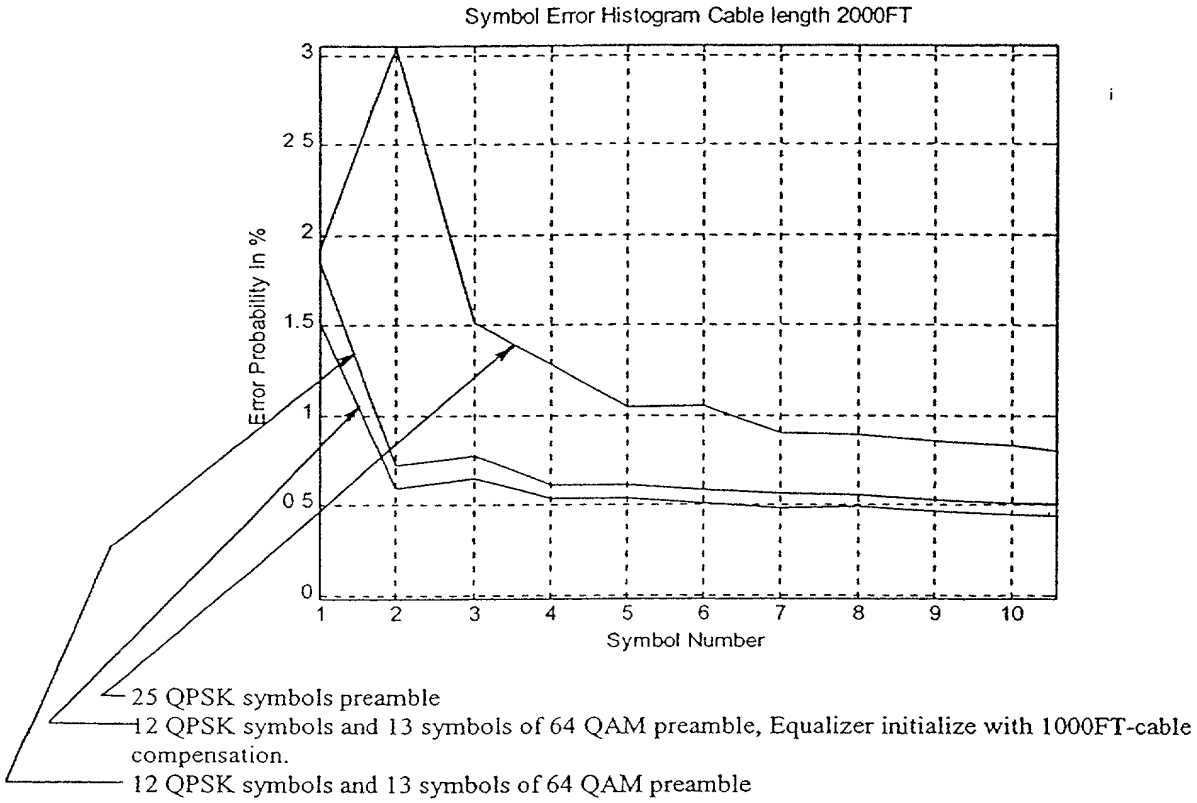


Figure 6

Cable Length	BER with Preamble Type 1	BER with Preamble Type 2	RS Error Rate with Preamble Type 1	RS Error Rate with Preamble Type 2
1000FT	5.42e-4	4.22e-4	6e-6	No Error over a million bursts.
2000FT	8.88e-4	6.55e-4	1.2e-4	1.6e-5

Figure 7

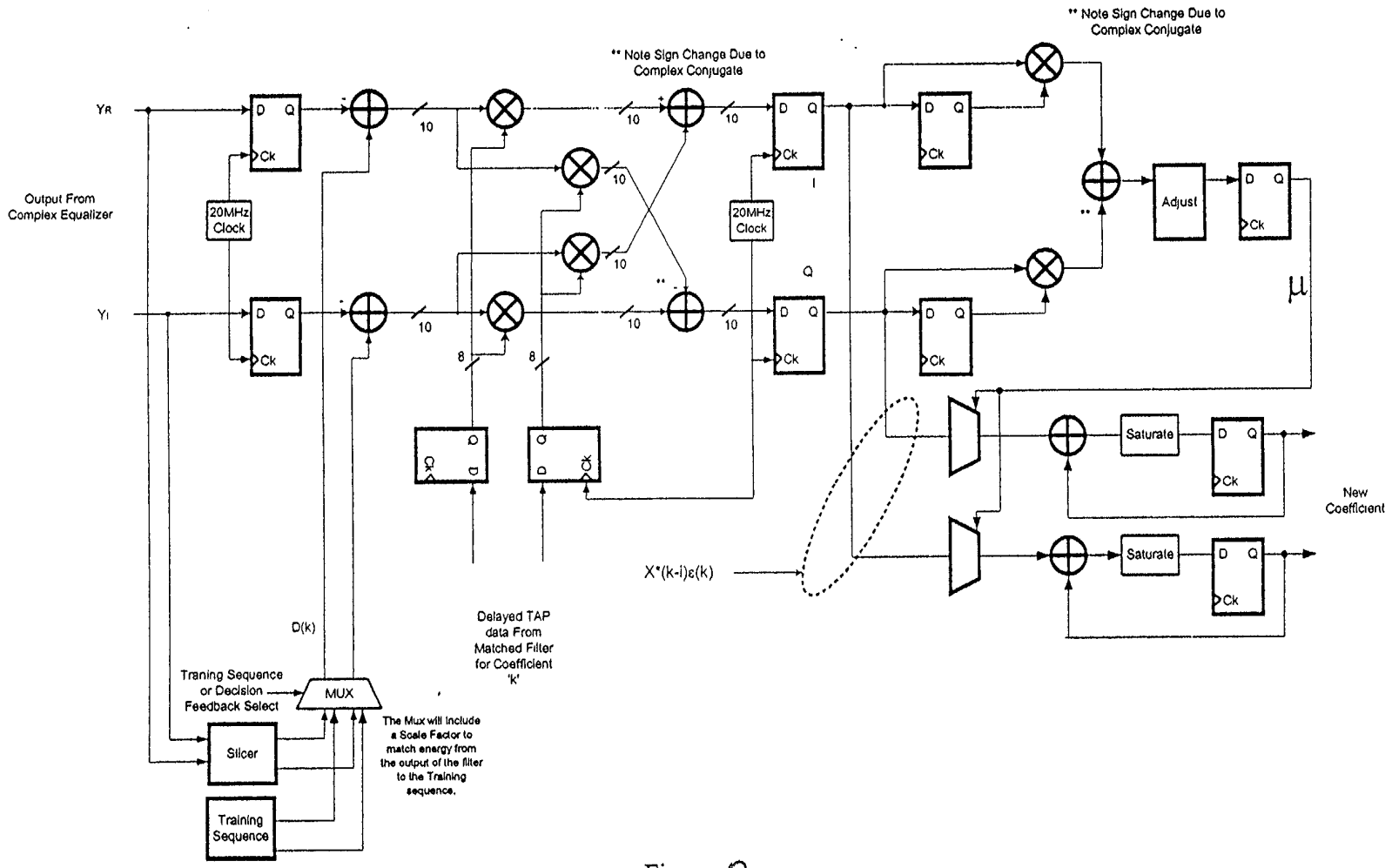
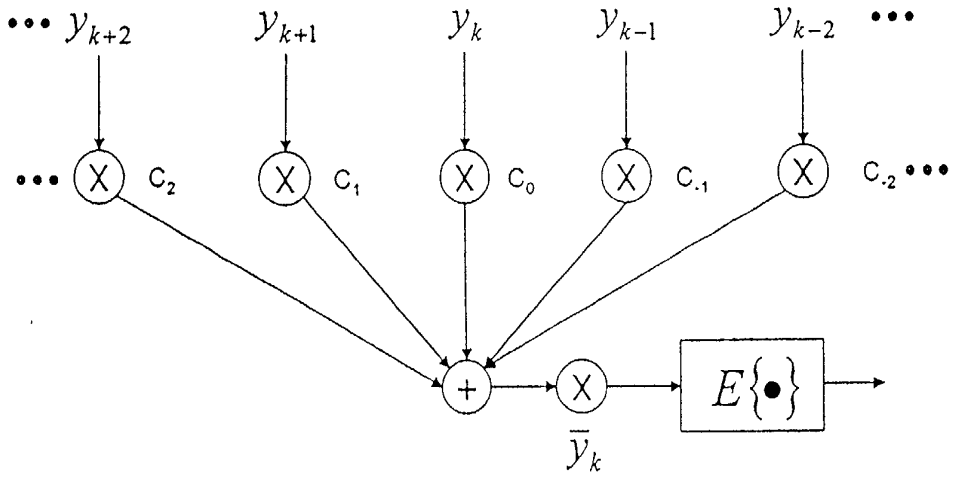
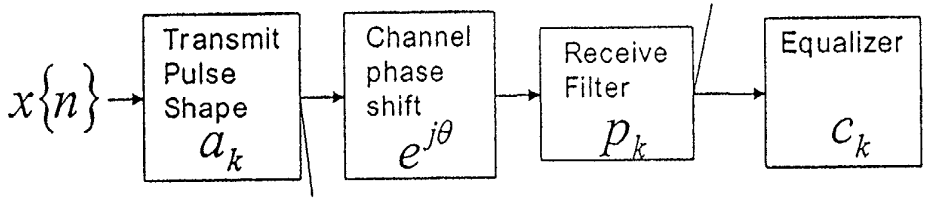

** Note Sign Change Due to Complex Conjugate
** Note Sign Change Due to Complex Conjugate
YR
YI
Output From Complex Equalizer
20MHz Clock
20MHz Clock
D Q
Ck
10
8
Adjust
Saturate
Saturate
New Coefficient
μ
X*(k-i)ε(k)
D(k)
Delayed TAP data From Matched Filter for Coefficient 'k'
Traning Sequence or Decision Feedback Select
MUX
Slicer
Training Sequence
The Mux will include a Scale Factor to match energy from the output of the filter to the Training sequence.

Figure 8



$$y_k = e^{j\theta} \sum_{j=-2N}^{2N} x_{k-j} h_j,$$

$$h_k = a_k * p_k$$



$$s_k = \sum_{j=-N}^{N} x_{k-j} a_j$$

Figure 9

FOS290' 89200860

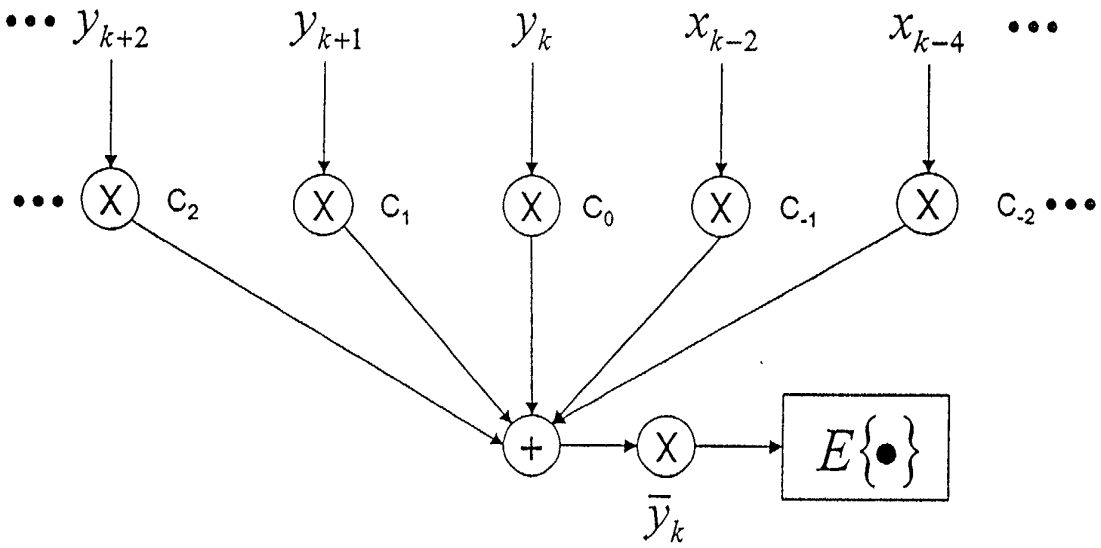


Figure 10

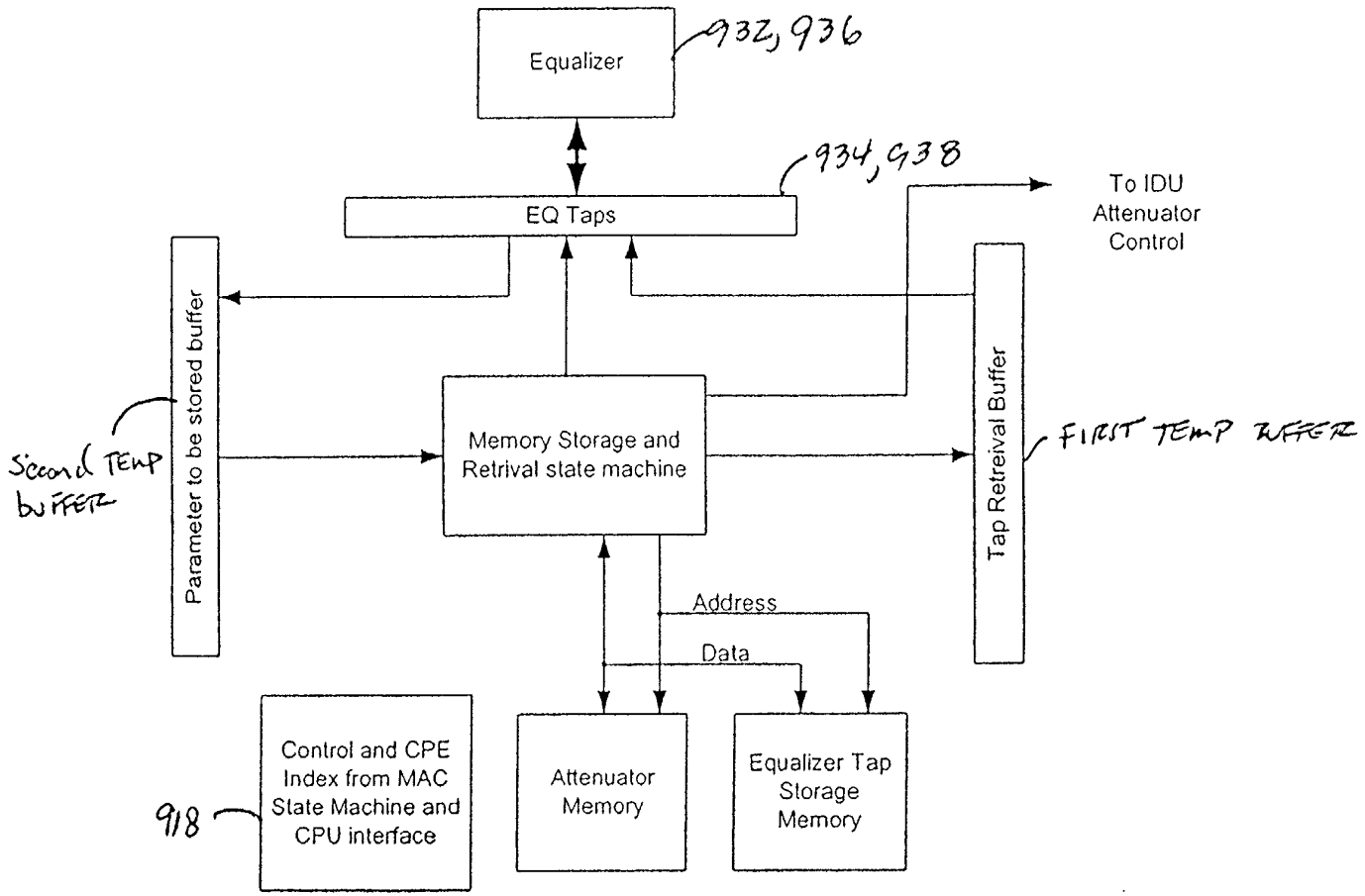

Equalizer
932, 936
934, 938
EQ Taps
To IDU Attenuator Control
Parameter to be stored buffer
Second TEMP BUFFER
Memory Storage and Retrival state machine
Tap Retreival Buffer
FIRST TEMP BUFFER
Address
Data
Control and CPE Index from MAC State Machine and CPU interface
918
Attenuator Memory
Equalizer Tap Storage Memory

FIGURE 11

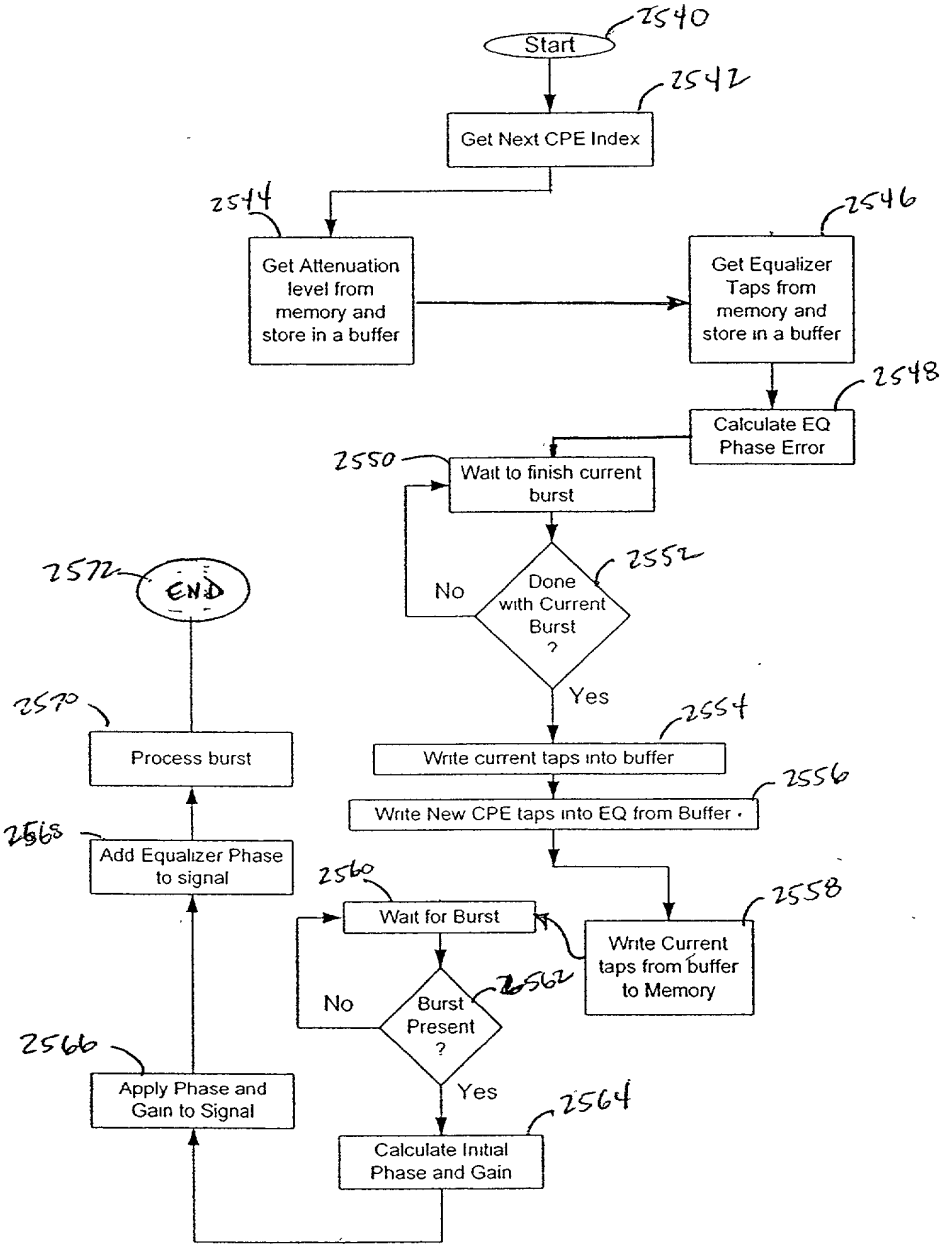

Start
2540
Get Next CPE Index
2542
Get Attenuation level from memory and store in a buffer
2544
Get Equalizer Taps from memory and store in a buffer
2546
Calculate EQ Phase Error
2548
Wait to finish current burst
2550
Done with Current Burst ?
2552
No
Yes
Write current taps into buffer
2554
Write New CPE taps into EQ from Buffer
2556
Write Current taps from buffer to Memory
2558
Wait for Burst
2560
Burst Present ?
2562
No
Yes
Calculate Initial Phase and Gain
2564
Apply Phase and Gain to Signal
2566
Add Equalizer Phase to signal
2568
Process burst
2570
END
2572

FIGURE 12

DIGITAL EQUALIZATION PARAMETER STORAGE AND RECOVERY

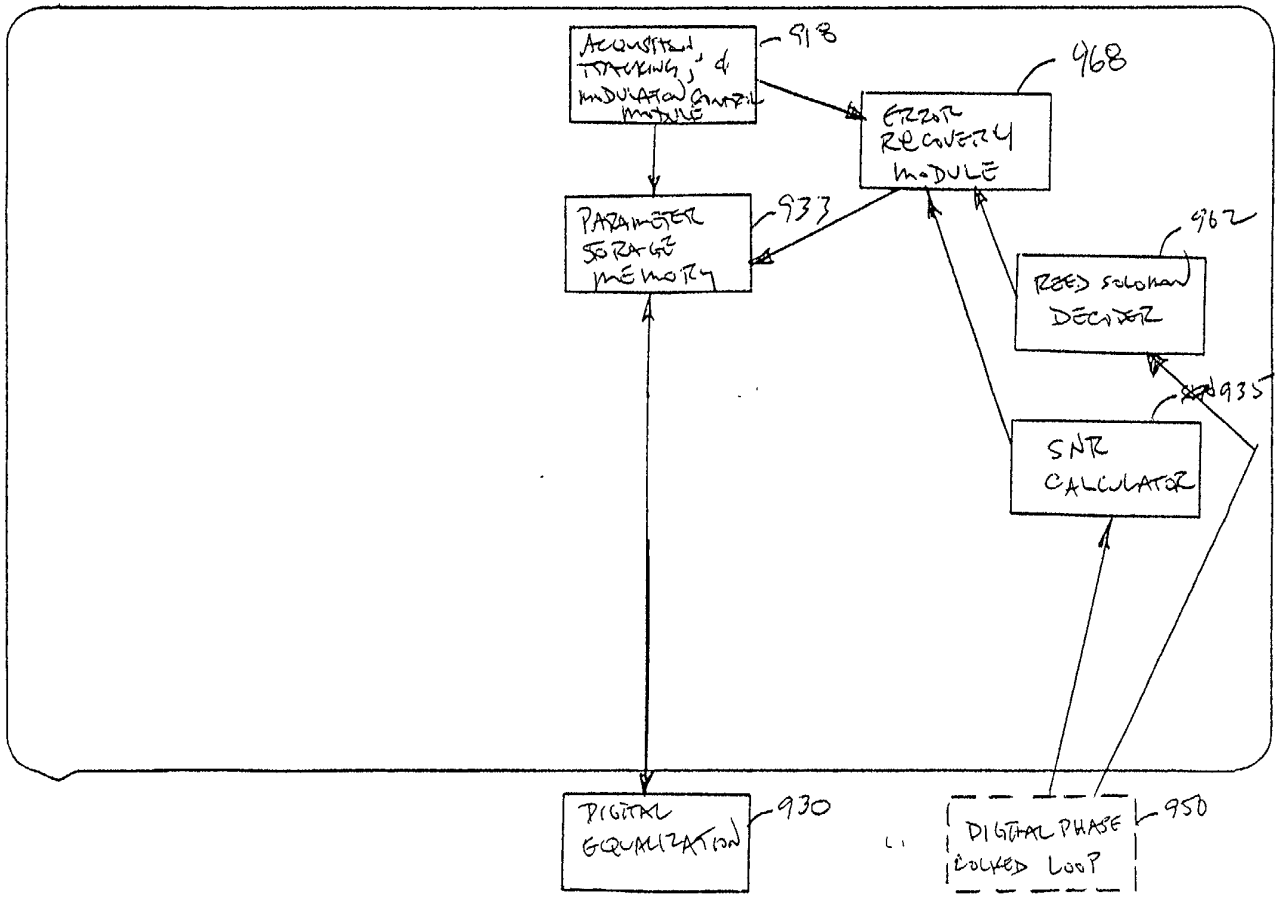


FIG. 13

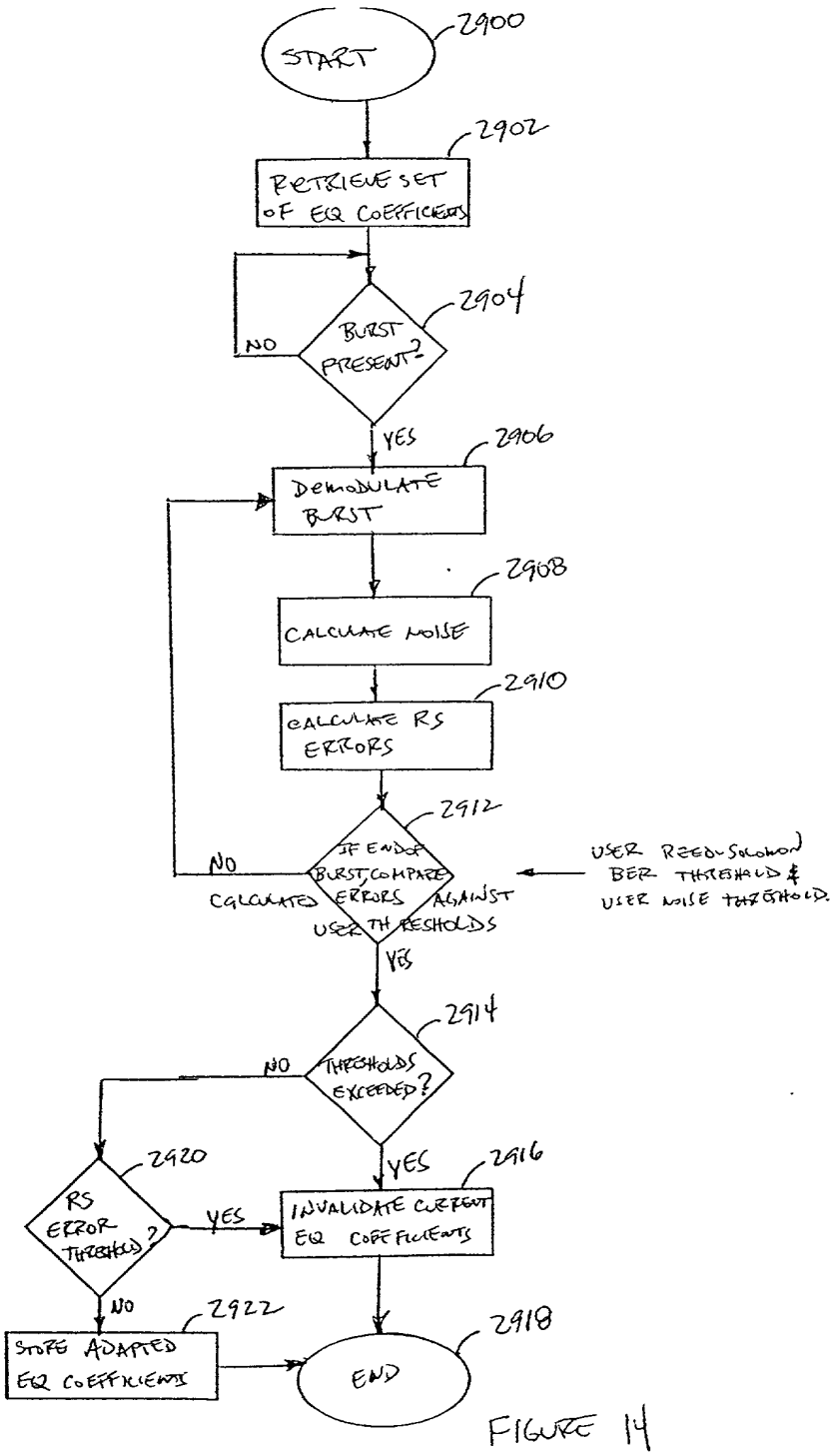

START
2900
RETRIEVE SET OF EQ COEFFICIENTS
2902
BURST PRESENT?
2904
NO
YES
DEMODULATE BURST
2906
CALCULATE NOISE
2908
CALCULATE RS ERRORS
2910
IF END OF BURST, COMPARE CALCULATED ERRORS AGAINST USER THRESHOLDS
2912
NO
YES
USER REED-SOLOMON BER THRESHOLD & USER NOISE THRESHOLD.
THRESHOLDS EXCEEDED?
2914
NO
YES
RS ERROR THRESHOLD?
2920
YES
NO
INVALIDATE CURRENT EQ COEFFICIENTS
2916
STORE ADAPTED EQ COEFFICIENTS
2922
END
2918

FIGURE 14